PATENT ABSTRACTS OF JAPAN

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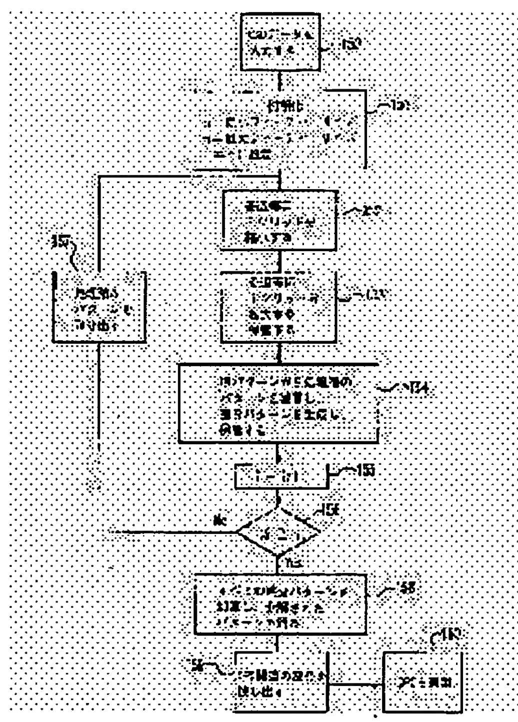
(54) **IMPROVED OPTICAL PROXIMITY CORRECTING SYSTEM**

(57)Abstract:

PROBLEM TO BE SOLVED: To improve its accuracy by previously deforming a mask, correcting only a feature important for one, and removing generation of the additional apex as many as possible in VLSI pattern transfer operation such as photolithography and reactive ion etching(RIE).

SOLUTION: This optical proximity correcting(OPC) method breaks down complicated computer aided design(CAD) data for a lithographic mask or a reticle into a basic quadrangular combination by using a series of reducing, enlarging and subtracting operations. In more detail, this OPC method discriminates plural gate areas in CAD design in the first place. Plural design shapes in the CAD design are sorted according to a geometric type. The sorted plural design shapes have at least one side in common with a second design shape. The sorted design shapes are grouped with its rear width as a reference. Lately, they are discriminated as gate areas, and all the grouped design shapes are corrected according to an applicable OPC rule.



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CLAIMS

[Claim(s)]
[Claim 1] It is the optical contiguity amendment approach for controlling the accuracy in VLSI patternizing actuation (a). The step which inputs the original design data set of a chip design, (b) The step which performs the decomposition procedure which includes a series of contraction, expansion, and actuation of subtraction in the level of said input design-data set, and sorts two or more design configurations in said design data set according to a geometric type, (c) Step which discovers and identifies for a design the part to which the design data set which is an important field relates (d) Approach containing the step which applies the optical contiguity amendment which changes the configuration of the part identified as it is a field important for a design.
[Claim 2] The step which performs a decomposition procedure to said input design-data set (a) The step to which only the specified quantity equal to the minimum feature size in the level of said design makes the 1st pattern reduce, (b) The step which only said specified quantity expands said pattern with which contraction was performed, and obtains the 2nd pattern, (c) Step which subtracts said 2nd pattern from said 1st pattern, and obtains the pattern of difference (d) The optical contiguity amendment approach containing the step which makes the step of said contraction, expansion, and subtraction repeat until it reaches the greatest feature size according to claim 1.
[Claim 3] the step which performs a decomposition procedure to said input design-data set -- difference -- the optical contiguity amendment approach according to claim 2 which is made to combine a pattern and contains further the step which obtains the design into which said Hara design data set was disassembled.
[Claim 4] The optical contiguity amendment approach according to claim 2 which contains the step which uses Boolean operation in order that said step which discovers and identifies a related part may discover an important feature on the basis of the crossover with front design level or next design level.
[Claim 5] The optical contiguity amendment approach according to claim 2 that said step which discovers and identifies a related part contains the step which identifies an important feature by proximity with other configurations on the same design level or other design level.
[Claim 6] In order to control accuracy in VLSI patternizing actuation, it is the system which carries out optical contiguity amendment to a chip design (a). The graphics design means for generating the original design data set of a chip design, (b) Contraction of a single string [level / of said Hara design data set], expansion, And perform a decomposition procedure including a subtraction operation and said design data set is sorted in two or more design configurations according to a geometric type. A configuration processor means to discover and identify for a design the part to which a ****** data set relates in an important field (c) System including an after-treatment equipment means to apply the optical contiguity amendment which changes the configuration of the part identified as it is a field important for a design.
[Claim 7] Said configuration processor means is programmed and only a predetermined amount equal to the minimum feature size of said design level reduces the 1st pattern. Next, carry out [aforementioned] specified quantity expansion of the reduced pattern, and the 2nd pattern is obtained. A series of actuation of obtaining a pattern is repeated. next, said 1st pattern to said 2nd pattern -- subtracting -- difference -- Furthermore, the system which carries out optical contiguity amendment to a chip design in order to control the accuracy in VLSI patternizing actuation according to claim 6 which repeats contraction, expansion, and actuation of subtraction until it reaches the maximum feature size.
[Claim 8] said configuration processor means -- said difference -- the system which carries out optical contiguity amendment to a chip design in order to control the accuracy in VLSI patternizing actuation according to claim 7 which is programmed further to combine a pattern and obtains the design into which said Hara design data set was disassembled.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is related to improvement in the accuracy of the image on lithography which uses optical contiguity amendment (OPC) for a detail more, and the image by which reactive ion etching (RIE) was carried out generally with regards to manufacture of a very-large-scale-integrated-circuit (VLSI) circuit element.
[0002]
[Description of the Prior Art] Manufacture of a semiconductor device depends for the pattern of computer-aided-design (CAD) generation on reproducing correctly on the front face of a component substrate. Generally this process of reproduction is performed by optical lithography, and various subtractive (etching) and additive (adhesion) processes continue after that. This photo mask has the image to which the computer generation pattern etched into the metal layer was expanded including patternizing of optical lithography irradiating the quartz plate with which the well-known metal was covered as a photo mask. Size is reduced on the substrate of a component and this irradiated image is patternized on a photographic sensitive film. The image formed on a component substrate of interference which takes place between pattern imprints, and the effect of a process changes from the ideal dimension and ideal form of an image which are expressed by the computer image. Depending on the property of a pattern, it depends for these change on the versatility of process conditions at coincidence. Since these change may affect the engine performance of a semiconductor device greatly, many approaches which focused on the CAD amendment system which generates an ideal image certainly have been investigated.
[0003] The advanced improvement in the engine performance of a VLSI circuit (namely, dimension contraction of a circuit to improvement in a rate) comes to be increasingly restricted by lack of the accuracy of the pattern in a series of lithography processes and RIE processes under a small dimension (for example, 0.5 micrometers or less). At the process of a photolithography, a pattern is imprinted from a photo mask by the photosensitive film on a wafer (resist). At a RIE process, this pattern in a resist is imprinted on the film of the variety on a wafer substrate.
[0004] The method of replacing a process with very high effective resolution with developing spending much gold is carrying out bias of the configuration of a mask pattern alternatively, as distortion of the pattern generated between wafer processings is compensated, i.e., it is what the configuration of a pattern is changed for so that distortion of a pattern may be compensated as a result (a pattern configuration is made distorted beforehand). This is performed by shifting the edge or the side of a pattern (change). Although it is generally used in order that the vocabulary of optical contiguity amendment (OPC) may express this process that carries out bias of the mask alternatively, this vocabulary tends to include amendment of pattern distortion which is not related to an optical image imprint. Generally the view which carries out bias of the pattern in order to amend the inaccuracy of an image imprint is applied to electron beam lithography, and in the both sides of the electron beam writing of a photograph mask, and direct wafer write-in actuation, it is used in order to lessen effect of a back scattering electron. For example, please refer to U.S. Pat. No. 5,278,421.
[0005] OPC extends application of the automatic view of pattern bias to two main pattern imprint processes adopted with the VLSI technique. First, one is classified as amendment "based on a regulation (rules-based)", by this approach, a pattern is sorted in a computer-aided-design (CAD) data set based on the regulation which associates the amount of bias to the magnitude of a pattern, a contiguity situation, and a pattern attribute like a consistency, and current operation of OPC is amended. And another is classified as amendment "based on collapsing (convolution-based)", and bias of the CAD pattern is carried out based on a specific pattern environment by this approach. a regulation function -- and it collapses and the both sides of a function can generate either a process simulation or experiential data. As an example of OPC operation "based on a regulation" (1) Richard C.Henderson and Oberdan "CD data requirementsfor proximity effect corrections" by W.Otto, 14th(s) Annual BACUS Symposium on Photomask Technology and Management, WilliamL.Brodsky and Gilbert Proc.SPIE depended on the volume on V.Shelden 2322 (1994), Pages 218-228 and (2) Oberdan W.Otto,

Joseph G.Garofalo, KKLow, Chi-Min Yuan, Richard C.Henderson, Christphe Pierrat, Robert L.Kostelak, Shiela Vaidya and "Automated optical proximity correction--a rules-based approach" by P.KVasudev, Optical/Laser Microlithography VII, Timothy Please refer to the volume on A.Brunner, Proc.SPIE2197 (1994), and pages 278-293. As an example of OPC operation "based on collapsing" (1) John P.Stirniman and Michael "Fastproximity correlation with zone sampling" by L.Rieger, Optical/Laser Microlithography VII, Timothy The volume on A.Brunner, Proc. SPIE2197 (1994), Pages 294-301 and (2) John Stirniman and Michael "Optimizing proximity correction for wafer fabrication proesses" by Rieger, 14th(s) Annual BACUS Symposium on Photomask Technology and Management, William The volume L.Brodsky and on GilbertV.Sheldem, Proc.SPIE Please refer to 2322 (1994) and pages 239-246. The common property of these operations that relate to this invention most is treated as a set of a rather geometric configuration as a design by which CAD data's define the function of a component.

[0006] There are two big faults with a current operation gestalt. As a result used as criteria which perform accuracy of a pattern duplicate correctly [OPC] rather than an improvement of a component function also in any of lithography or a RIE process, I hear that much unnecessary amendments are needed, and there is the 1st fault. Without making worth of a VLSI chip increase in any way, this complicates a CAD data set and the design Ruhr inspection deck, makes the amount of CAD data, mask writer data, and the inspection tool data that reach increase, and makes the cost of an OPC process increase. Such a thing is being able to say also to the two-dimensional amendment treating the phenomenon the angle (corner's) section's having a radius of circle in amendment of wiring width of face also to the 1-dimensional amendment which focused. With regards to the addition of the new top-most vertices (a folding point and salient point) to a CAD layout, this makes the amount of data increase greatly, and the 2nd fault complicates mask inspection. The target of an efficient OPC procedure must be minimum-izing the top-most vertices added in an amendment process.

[0007]

[Problem(s) to be Solved by the Invention] Therefore, the purpose of this invention is offering the approach for improving the effectiveness of an OPC process, i.e., the ratio of cost and profits nature, and equipment. Another purpose of this invention is offering the OPC procedure of amending only an important feature and removing generating of additional top-most vertices as much as possible. Furthermore, the specific purpose of this invention is offering the contiguity amendment procedure which is timely and amends by the good approach of cost efficiency based on a realistic data set, without making the amount of data increase superfluously.

[0008]

[Means for Solving the Problem] According to this invention, the approach and equipment of the improved optical contiguity amendment are offered, and this carries out bias of the part with important design level, without making the amount of data which defines the circuit increase too much. This invention improves the effectiveness of OPC in a VLSI production process by realizing a hierarchical design Ruhr inspection (DRC) system with a fundamental CAD system, supporting Boolean operation, and identifying, the feature, i.e., the pattern part, functionally related before pattern compensation. This invention is based on the simple geometric actuation for separating the edge which exists during a CAD layout, and enables bias actuation of a feature without the addition of new top-most vertices.

[0009] Furthermore, this invention disassembles CAD pattern data into the fundamental square which touches the top-most vertices which exist in a original design at a detail using a series of contraction, expansions, and subtraction actuation. Thus, next, the defined square is classified based on those functional relevance on the basis of the spatial relation of those squares to the level in front of CAD design level, or next level. By shifting the edge of only a fundamental square expected to be related to improvement in a VLSI component function, generation of new top-most vertices is minimum-ized, and a required activity is made only to the high added value part of a circuit design. the operation gestalt in which an actual contiguity classification and bias are existing -- the same -- a regulation -- it collapses and is carried out based on functions or some of these combination.

[0010] In a specific example, two or more gate fields under CAD design are identified first. Two or more design configurations under CAD design are sorted according to a geometric type. The design configuration by which plurality was sorted is sharing the 2nd design configuration and at least 1 side face. Grouping of the sorted design configuration is carried out on the basis of width of face after that. Finally, based on an available OPC regulation, bias of all the design configurations that were identified as a gate field and by which grouping was carried out is carried out.

[0011]

[Embodiment of the Invention] If drawing is referred to here, the example of the gate level of a CMOS device is shown especially in drawing 1 . The important field is shown by the crossover field of the configuration which has demarcated the polycrystal silicon-gates 11, 12, 13, and 14, and the configurations 15 and 16 which have demarcated the diffusion field. Two patterns are the same if only the design of polycrystal silicon-gate level is seen. However, when the knowledge of a diffusion location is considered, contiguity amendment with a left layout is restricted to three vertical lines 17, 18, and 19, and, on the other hand, it turns out with a right-hand side layout that it is necessary to amend the pattern 20 of a more complicated U character mold.

[0012] Drawing 2 shows another example of the gate level of a CMOS device, and the two important angle (corner) sections 21 and 22 in the diffusion field 23 are shown here. In a two-dimensional OPC procedure, in order to negate the radius-of-circle effectiveness of a corner, an edge ornament (serif), i.e., words, is used. In the polygon which shows the diffusion field 23, only the corners 21 and 22 to which a corner also comes a radius of circle suddenly, and superposition tolerance becomes small are related to OPC.
[0013] the OPC procedure according to this invention – from the procedure of three sorts and one bias – changing – here – the gate – it is explained using the example of conductor (GC) level. The 1st sort procedure discovers all the activity gate fields under polycrystalline silicon design as a field where GC level configuration intersects the diffusion level configuration. The 2nd sort procedure is made into the geometry (many are squares) which divides a design data independently and carries out termination in the folding point (for example, 30 of drawing 3 , 32) of an existing straight line, or a linear endpoint. This geometric sorting is performed by a series of contraction, expansion, and actuation of subtraction. Contraction actuation removes all configurations smaller than the appointed contraction parameter (irrespective of [whether it is an independent configuration or it is geometric add-on]). Expansion actuation restores the data after removal to each original size. What subtracted this new data set from the original polycrystalline silicon design serves as a configuration with specific width of face. Data are separable into the geometry to which size increases and goes by repeating these contraction, expansion, and actuation of subtraction over the whole range of a contraction value. Since change of feature size should be generated in the folding point where it is [in a design data] existing, the boundary of these configurations is in agreement on an existing folding point. Only the geometry which is actually in agreement chooses the last sort actuation as the activity gate field discovered by the 1st sort actuation. the bias actuation of change feature size into "the configuration which include the gate" here make the minimum the number of additional top-most vertices without the possibility of break a design regulation, first by move the vector of geometry to the point that at least one top-most vertices exist in a original design by carry out the bias of the whole activity gate field (shift an edge).
[0014] This invention is illustrated using an example. It assumes disassembling a pattern as shown in drawing 3 into a fundamental square. Pattern A, a call, and this should be obtained from the CAD data set of the VLSI circuit design under processing in this pattern. The minimum feature pattern size considers as a part for two grids of a design, and assumes the greatest feature pattern size to be a part for ten grids of a design. Contraction actuation to which Pattern A makes a pattern reduce by 2 design grid for every side as shown in drawing 4 is performed. Width of face is reduced to the line of 0, and two parts of the pattern in 41 and 42 are lost from a CAD layout. After contraction actuation, for every side, this pattern is expanded by 2 design grid, and is returned. All the patterns that remained by contraction actuation are called Pattern B to the original size of them return and here, as drawing 5 shows. Next, by subtracting Pattern B (drawing 5) from Pattern A (drawing 3), the pattern of difference as shown in drawing 6 is obtained. It turns out that the patterns of this difference are two lines 41 and 42 lost in the first contraction actuation.
[0015] As for the pattern B shown in drawing 5 , contraction actuation to which 3 design grid part pattern is made to reduce for every side as shown in drawing 7 R> 7 is performed next. Width of face is reduced to the line of 0, and two parts of the pattern again shown by 43 and 44 are lost by this actuation. Next, the pattern of the result is expanded by 3 design grid, is returned for every side, and turns into the pattern C shown in drawing 8 . the first difference shown by drawing 6 here – the 2nd difference by which the pattern subtracted Pattern C (drawing 8 R> 8), and was obtained from Pattern B (drawing 5) – it is added to a pattern and the pattern shown in drawing 9 is obtained. In addition to two lines 41 and 42 lost in the first contraction actuation, also notice two lines 43 and 44 lost in the 2nd contraction actuation about being contained in this pattern. Notice the group of these two lines also about having sorted in size effectually in the combination of these actuation.
[0016] Contraction actuation to which 4 design grid part pattern is made to reduce for every side is performed as the pattern C shown by drawing 8 is shown by drawing 1010 below. One part of the pattern shown in 45 is reduced to the line of width of face 0 this time. Next, the pattern obtained as a result is expanded by 4 design grid, and is returned for every side, and the pattern D shown in drawing 11 is obtained. the difference shown in drawing 9 here – the 3rd difference by which the sum of a pattern subtracts Pattern D (drawing 11), and is obtained from Pattern C (drawing 8) – it is added to a pattern and the pattern shown in drawing 12 R> 2 is obtained. Note that this pattern contains 45 lost in the 3rd contraction actuation in addition to the lines 41, 42, 43, and 44 lost in the first two contraction actuation. Be careful also of what the line was effectually sorted for by size in the combination of this actuation also here again. Since the greatest configuration size is assumed to be a part for 10 design grid, a repetition of the contraction procedure beyond this and an expansion procedure is unnecessary. The reason is that the contraction actuation for 5 design grid for every side is equal to the maximum feature size of 10 design grid.
[0017] the difference shown in drawing 12 here – if the sum of a pattern is added to Pattern D (drawing 11), that by which the original pattern was disassembled into the fundamental square will be obtained as shown in drawing 13 . In this example, the polycrystal silicon-gate, i.e., GC level, was decomposed into the simple square of a lot. The following step is choosing what should perform OPC from the square generated in the decomposition

procedure. In the crossover with these squares and front CAD level, and this case, this is performed by investigating the crossover with a diffusion field as shown in drawing 14 . Two squares 43 and 44 exist on the diffusion field 141, and these squares are chosen as what intersects a diffusion field. This is performed by Boolean operation and this operation is identified as that to which only two squares 43 and 44 intersect the diffusion field 141.

[0018] This procedure is summarized in the flow chart of drawing 15 . Original CAD data are inputted at step 150. A decomposition procedure is performed as the approximate account was carried out by the above to this CAD data set. Furthermore, speaking generally, it being decided by the greatest feature size that the minimum feature size of a CAD design is size's (a part's for 2 design grid [For example, the above-mentioned example]) as which the 1st is specified in advance, and it is the size's (a part's for 10 design grid [For example, the above-mentioned example]) as which the 2nd is specified in advance. This procedure determines n as the minimum feature size in functional block 151, makes m the maximum feature size, is further set up with i=n and is initialized. This procedure begins from a original design, repeats a majority of contraction, expansions, and subtraction, and obtains a series of patterns. First, as for a pattern, contraction actuation in functional block 152 is performed, and a pattern is reduced by i design grid for every side. With functional block 153, a pattern is expanded by i design grid, and is returned [2nd] for every side, and a new pattern is obtained. This new pattern is kept temporarily. The pattern obtained with functional block 153 is subtracted from the input configuration to functional block 151 with functional block 154, and obtains the pattern of a difference. The pattern of this difference is kept temporarily here. In functional block 155, the increment only of 1 is carried out, i is the judgment block 156 after that, and the test which judges whether 2i is equal to m or larger than m is performed. if that is not right, the pattern generated with functional block 153 will be taken out with functional block 157, the loop back of this procedure will be carried out to functional block 152, and contraction actuation of functional block 152 and expansion actuation of functional block 153 will perform again the pattern generated with functional block 153 here -- having -- difference new after that at functional block 154 -- a pattern is generated. when the twice of an index number i are equal to m or becomes larger than m, it judges by the test in the judgment block 156 -- having -- functional block 158 -- all difference -- the pattern design which the pattern was combined and was decomposed is obtained. Generation of the decomposed pattern design discovers the decomposition pattern relevant to OPC with functional block 159. Boolean operation is performed and an important feature is discovered based on the crossover with front design level or next design level. Furthermore, proximity with other features on the same design level or other design level can also be used for classifying a part for the divided data division. The part relevant to OPC is discovered and OPC is performed into these parts by functional block 160.

[0019] Since, as for the pattern of the gate 12, a perpendicular part and a level part have the same line breadth in the case of the polycrystal silicon-gate 12 of drawing 1 , the gate 12 whole will be classified according to the sort process mentioned above as one pattern. Although the important field of the gate 12 is a field of the slash which lapped with the diffusion field 15, by OPC amendment, bias of it is carried out so that the edge or the side of not only the field of this slash but the vertical line 17 and the 18 whole may be shifted. Therefore, the flection or corner like 30 of drawing 3 and 32 does not arise by OPC amendment. In addition, since there are few degrees influenced by distortion, even if the field which is not [other than the slash field which lapped with the diffusion field] important receives the edge shift (distortion) by bias, it does not produce a problem. Although, as for the case of the pattern of drawing 3 , the fields 34 and 36 of a slash are separated as a pattern part in a sort process, respectively, since it dissociates as a square which uses flections 30 and 32 as an edge, a flection or a corner new as a result of the OPC amendment to fields 34 and 36 does not produce fields 34 and 36.

[0020] This invention is realizable on the hardware shown in drawing 16 . The original CAD design of a chip is generated by graphics design terminal unit 161 like an IBM6095 graphics design terminal unit. The data set generated with the terminal unit 161 is IBM. It is outputted to a workstation 162 like RISC6000 workstation. A workstation works as a configuration processor and decomposes a chip design first as mentioned above. A workstation performs OPC amendment to a data set after completing a decomposition procedure there. Thus, the amended data set is outputted, and is returned to a terminal unit 161, and OPC amendment is considered here. When it is judged that OPC amendment is considered and it can receive, a data set is IBM after that. It is outputted to a mainframe computer 163 like ES/9000 computer. After treatment which is needed for this main frame computer 163 preparing mask writer input data is performed.

[0021] This approach was adopted as manufacture of the gate level of 64Mb dynamic random access memory (DRAM), and reduction of 10% of data of it was completed compared with the case where bias only of the activity gate field is carried out.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the top view showing the field where the gate level of a CMOS device is important.
[Drawing 2] It is the top view showing the important angle (corner) point of participating in OPC, all over a polygonal diffusion field.
[Drawing 3] It is the top view showing an example of a pattern which encounters by the VLSI circuit design.
[Drawing 4] It is the top view of the pattern shown in drawing 3 to which contraction actuation was performed.
[Drawing 5] All the patterns that remained by contraction actuation are the top views of the pattern shown in drawing 4 expanded so that it might be restored to each first size.
[Drawing 6] It is the top view showing that by which the pattern of drawing 5 was subtracted from the first pattern shown in drawing 3 .
[Drawing 7] It is the top view of the pattern shown in drawing 5 to which contraction actuation was performed.
[Drawing 8] All the patterns that remained by contraction actuation are the top views of the pattern shown in drawing 7 expanded so that it might be restored to each first size.
[Drawing 9] It is a top view although the difference of the pattern shown in the pattern shown in drawing 6 at drawing 5 and drawing 8 was added.
[Drawing 10] It is the top view of the pattern shown in drawing 8 to which contraction actuation was performed.
[Drawing 11] All the patterns that remained by contraction actuation are the top views of the pattern shown in drawing 10 R> 0 expanded so that it might be restored to each first size.
[Drawing 12] It is the top view showing what added the difference of the pattern shown in the pattern shown in drawing 6 and drawing 9 at drawing 8 R> 8 and drawing 11 .
[Drawing 13] The configuration of the first pattern shown in drawing 3 is the top view showing what decomposed into the fundamental square.
[Drawing 14] It is the top view showing two squares generated during the selection procedure, i.e., a decomposition procedure, based on the crossover with said square and front CAD level.
[Drawing 15] It is the flow chart showing the basic method of this invention.
[Drawing 16] It is the block diagram showing the typical hardware which can carry out this invention.
[Description of Notations]
11, 12, 13, 14 Polycrystal silicon-gate
15, 16, 23 Diffusion field
17, 18, 19, 20 Field which needs contiguity amendment
21 22 The salient point which needs OPC amendment
41 42 Part lost in the first contraction actuation
43 44 Part lost in the 2nd contraction actuation
45 [ ] Part Lost in 3rd Contraction Actuation
141 [ ] Diffusion Field
161 [ ] Graphics Design Terminal Unit
162 [ ] Workstation
163 [ ] Mainframe Computer

[Translation done.]

* NOTICES *

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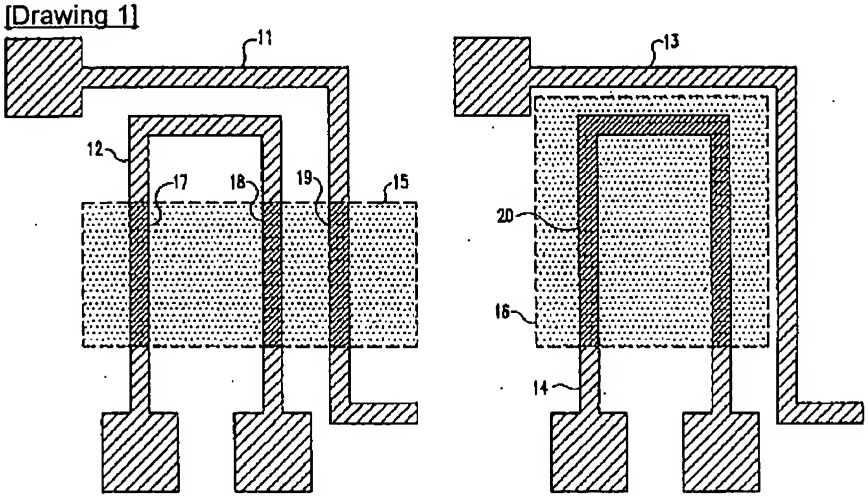
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



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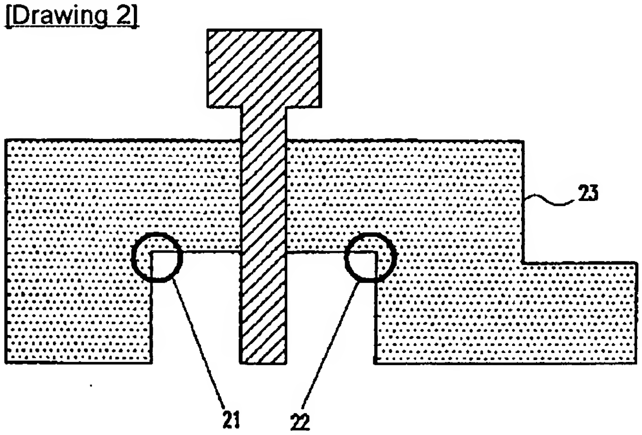

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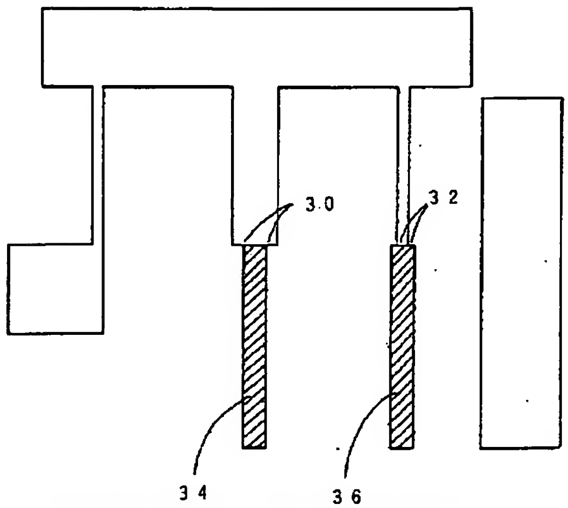

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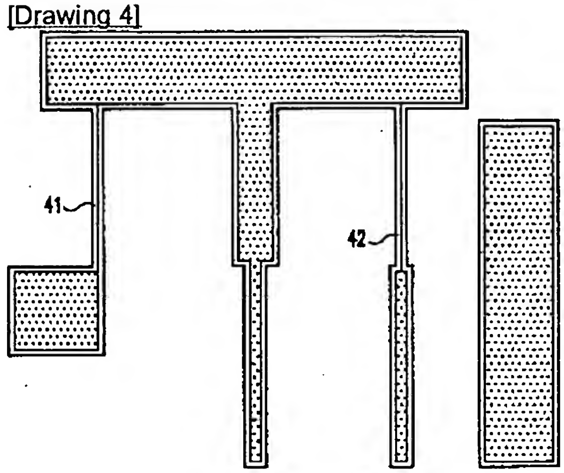

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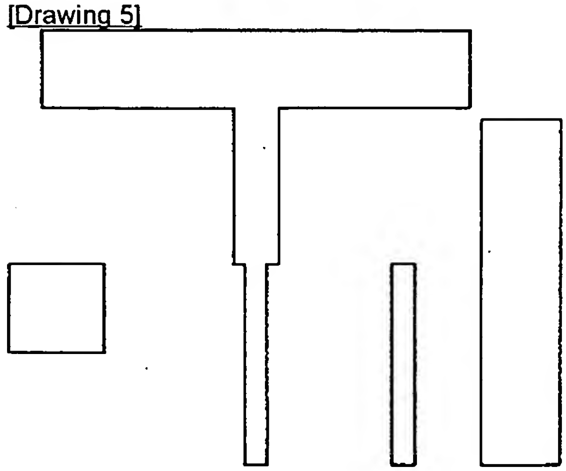

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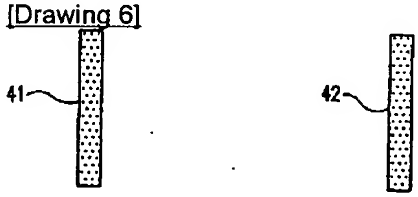

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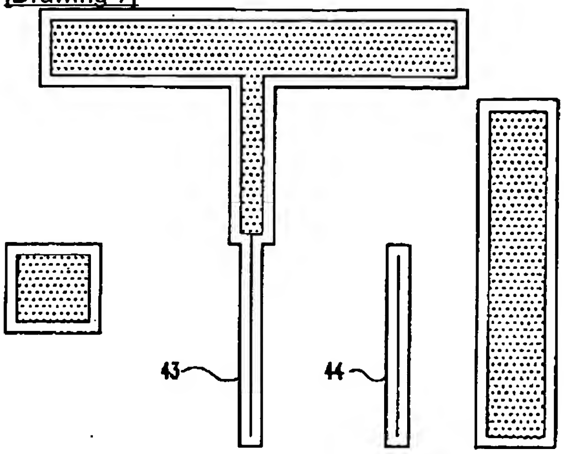
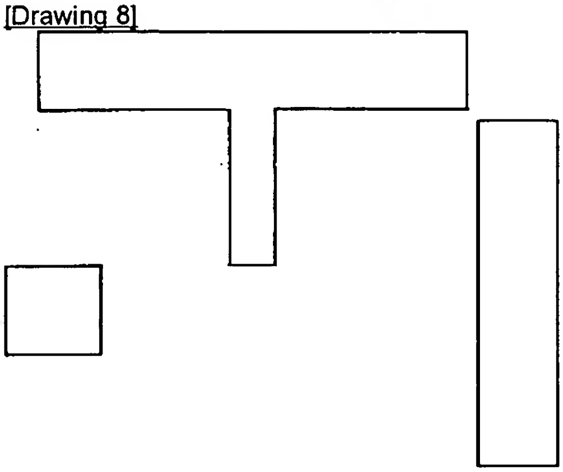
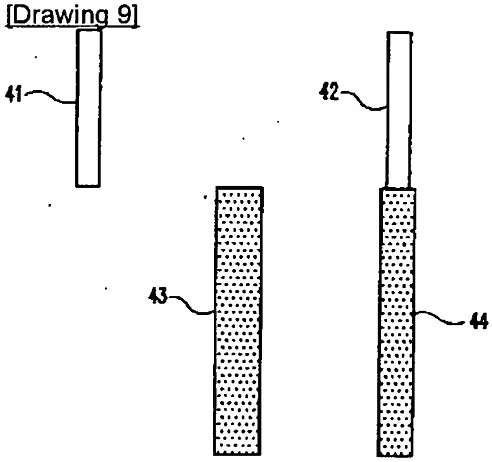


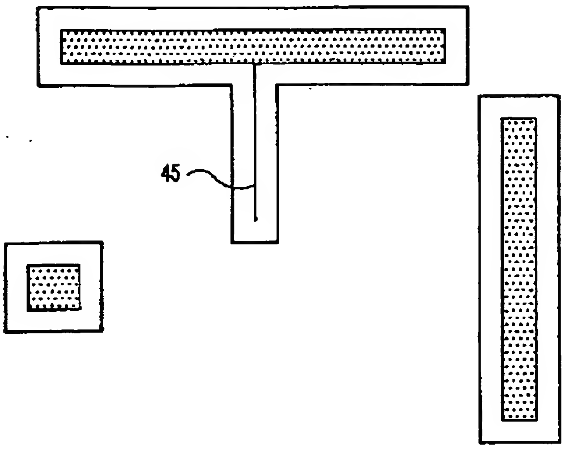
[Drawing 8]



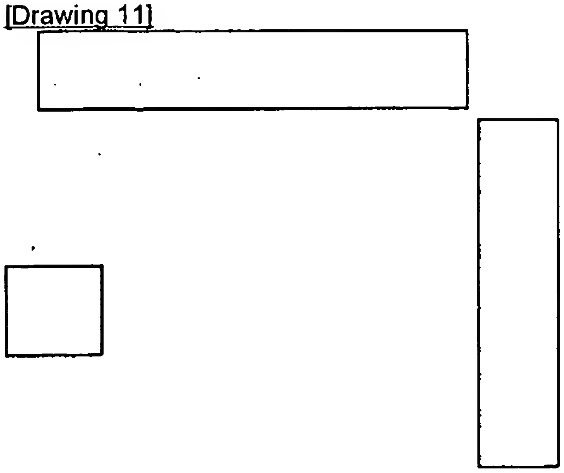
[Drawing 9]



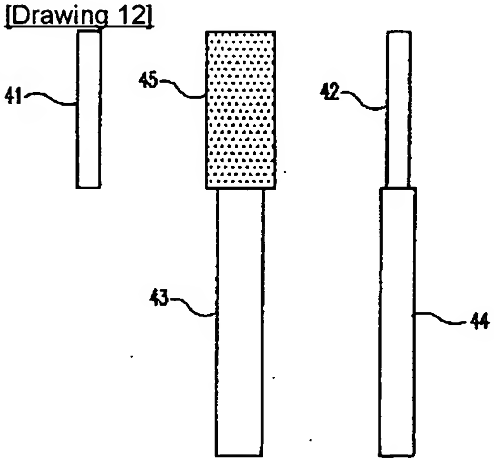
[Drawing 10]



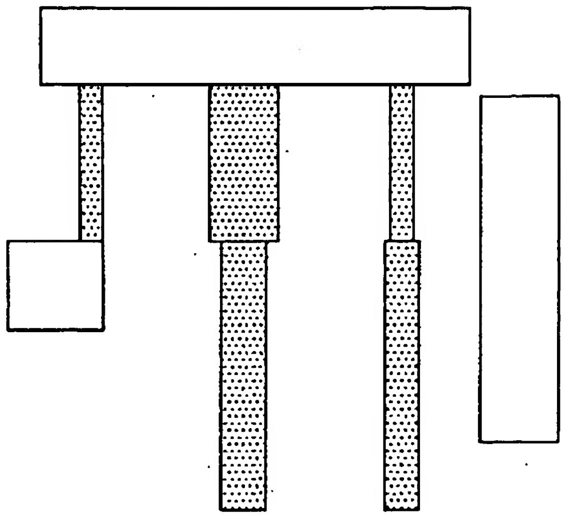
[Drawing 11]



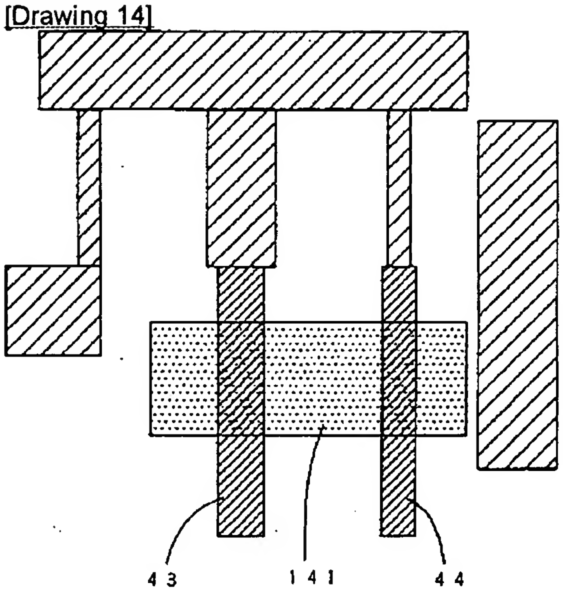
[Drawing 12]



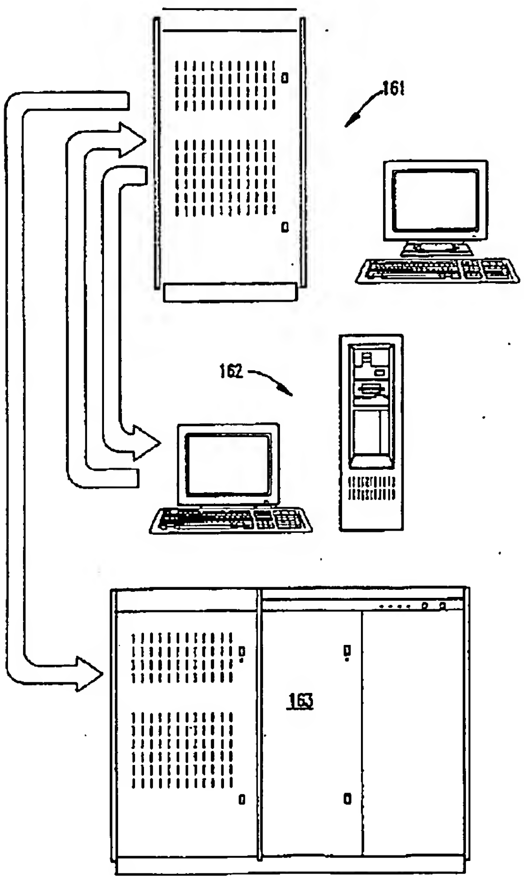
[Drawing 13]



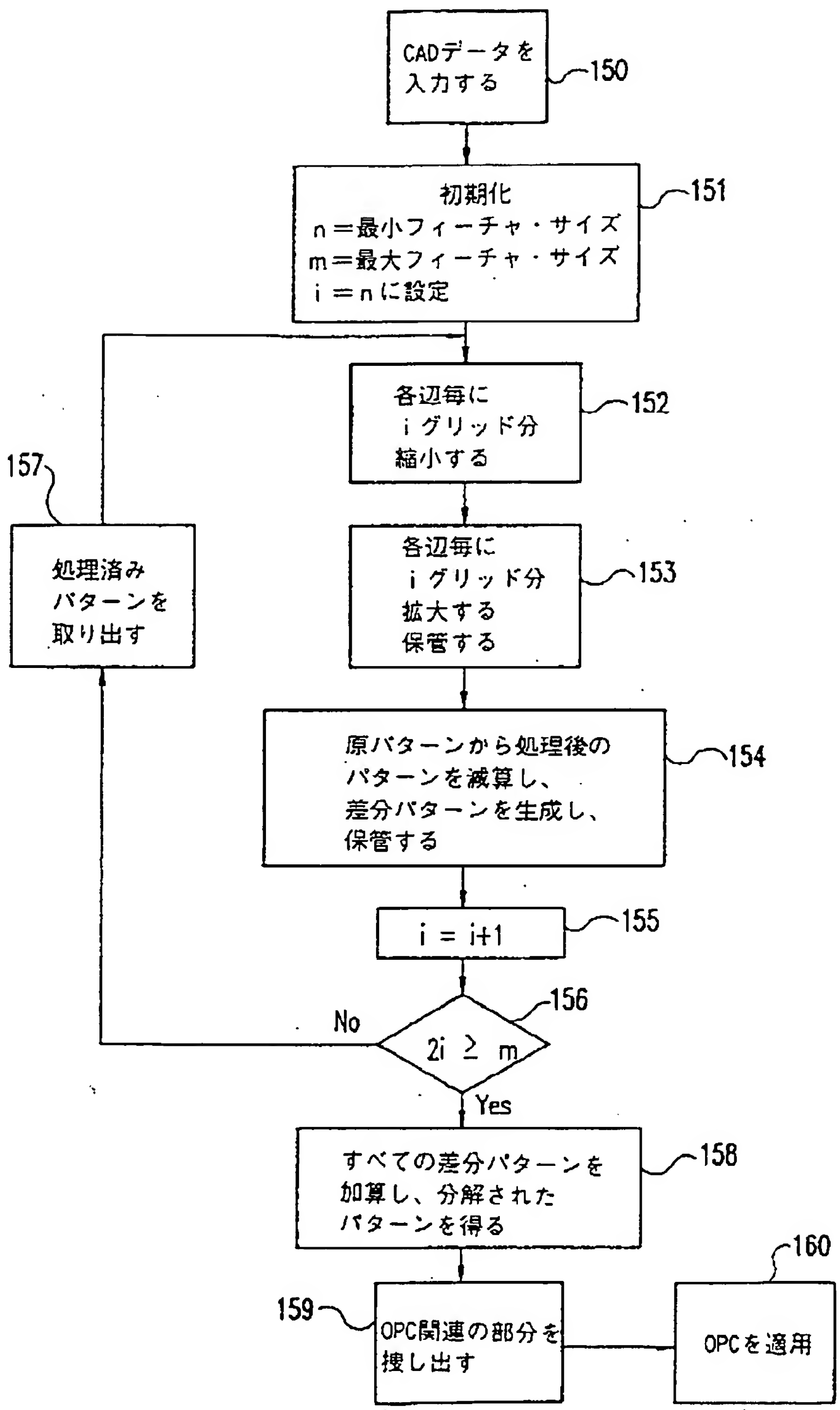
[Drawing 14]



[Drawing 16]



[Drawing 15]



[Translation done.]